

The diagram shows a PLL system. A reference signal s_P is input to a phase-locked loop (PLL) block 130. The output of block 130 is s_{FB} , which is fed back to the input of block 130. The output of block 130 is also fed into a power amplifier (PA) block 120. The output of block 120 is fed into a variable gain block 110, which is controlled by a microprocessor (μP) 180. The output of block 110 is s_M , which is fed into a summing junction. The summing junction also receives a signal from a phase shifter block 171. The output of the summing junction is fed into a phase-locked loop (PLL) block 103. The output of block 103 is s_{I2} , which is fed into a summing junction 101. The summing junction 101 also receives a signal s_{I1} . The output of block 101 is $s_{I'}$, which is fed into a phase-locked loop (PLL) block 160. The output of block 160 is $s_{Q'}$, which is fed into a summing junction 102. The summing junction 102 also receives a signal s_{Q1} . The output of block 102 is s_{Q2} , which is fed into a phase shifter block 172. The output of block 172 is fed into the summing junction 101. The output of block 172 is also fed into the summing junction 102. The output of block 172 is also fed into the summing junction 101. The output of block 172 is also fed into the summing junction 102.

Fig. 1 PRIOR ART

20250906092006

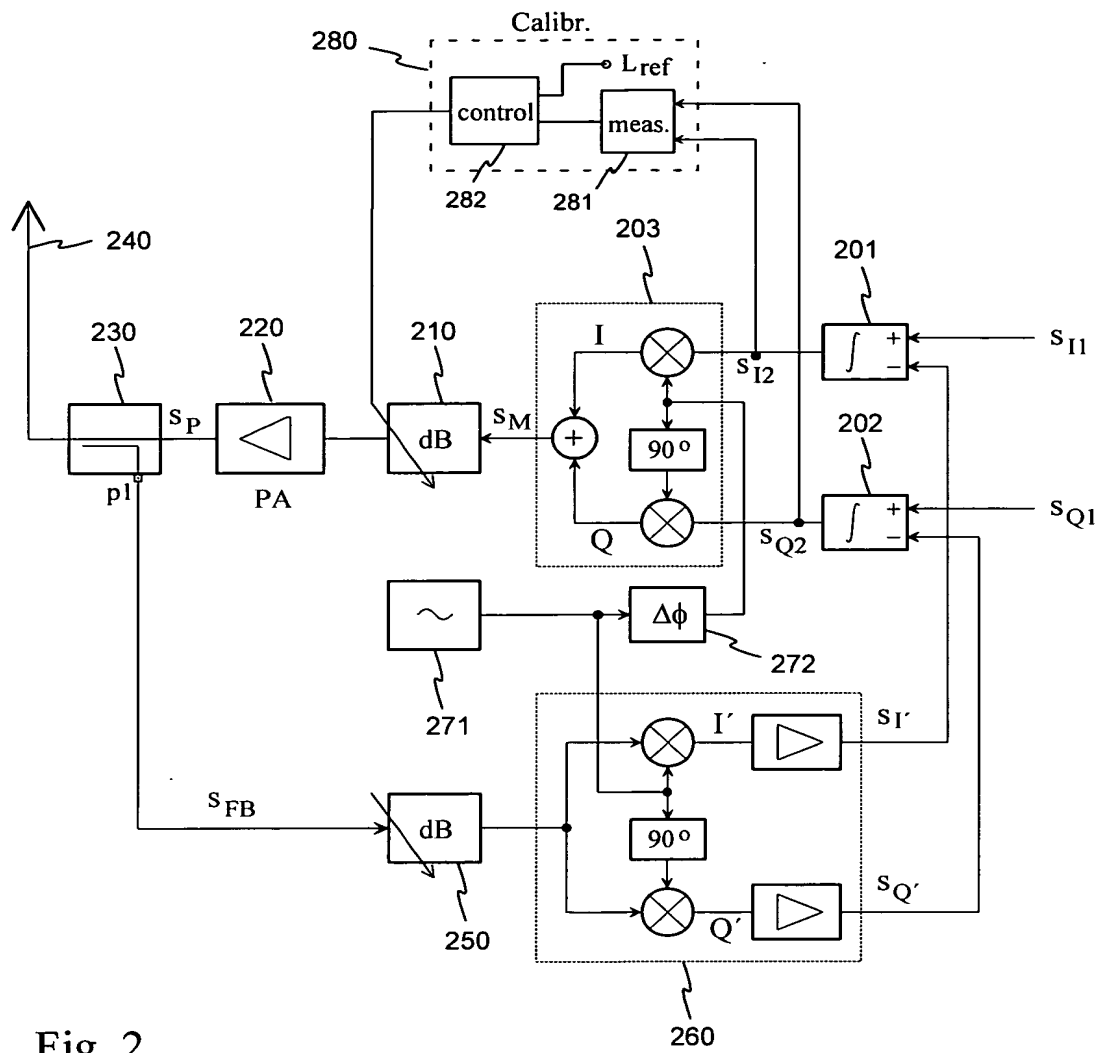


Fig. 2

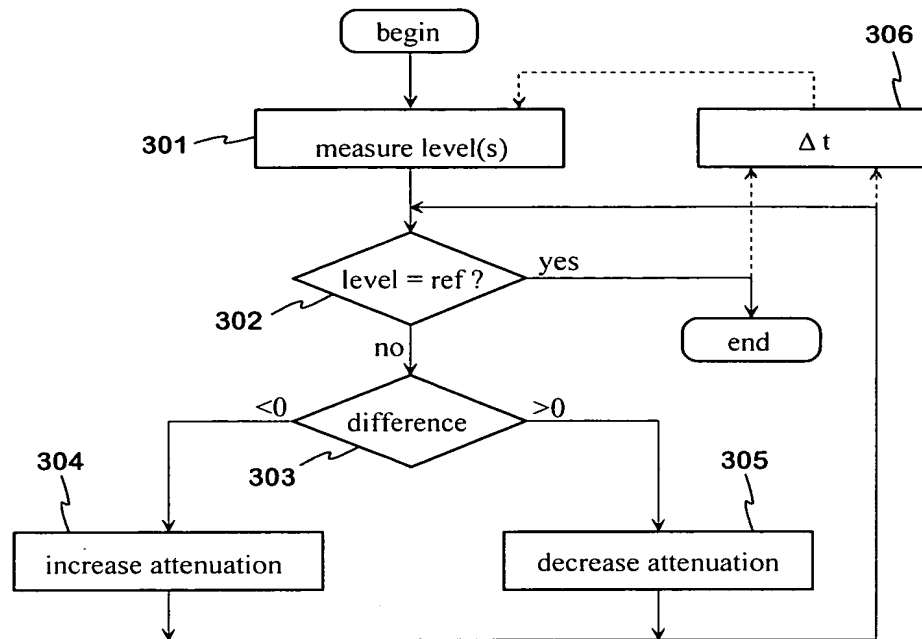


Fig. 3

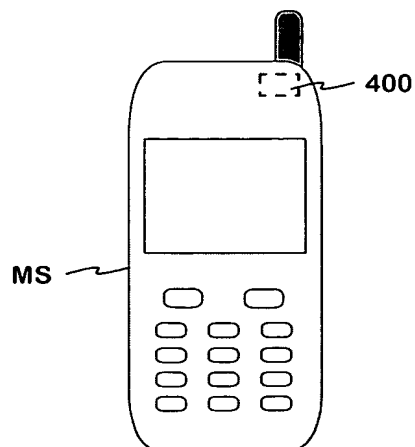


Fig. 4